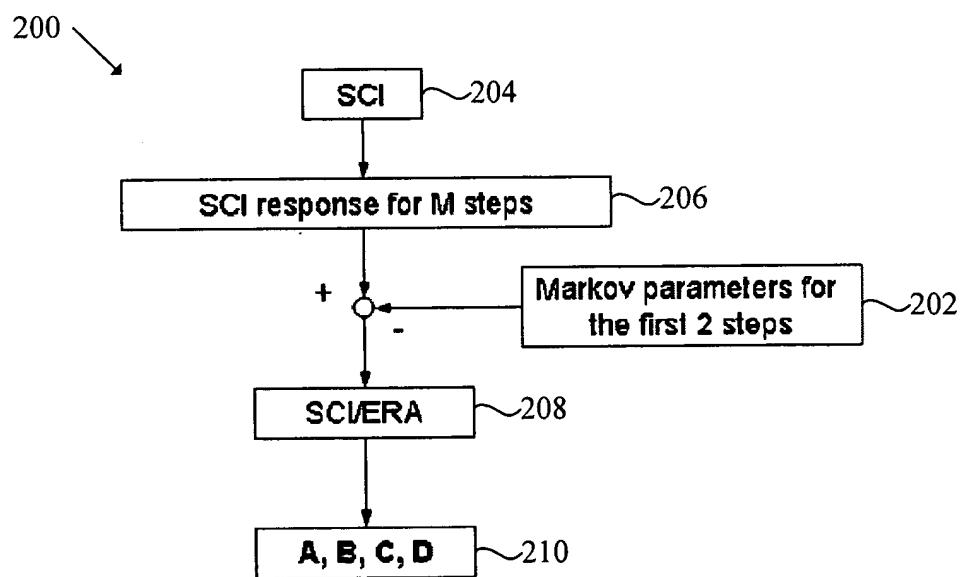
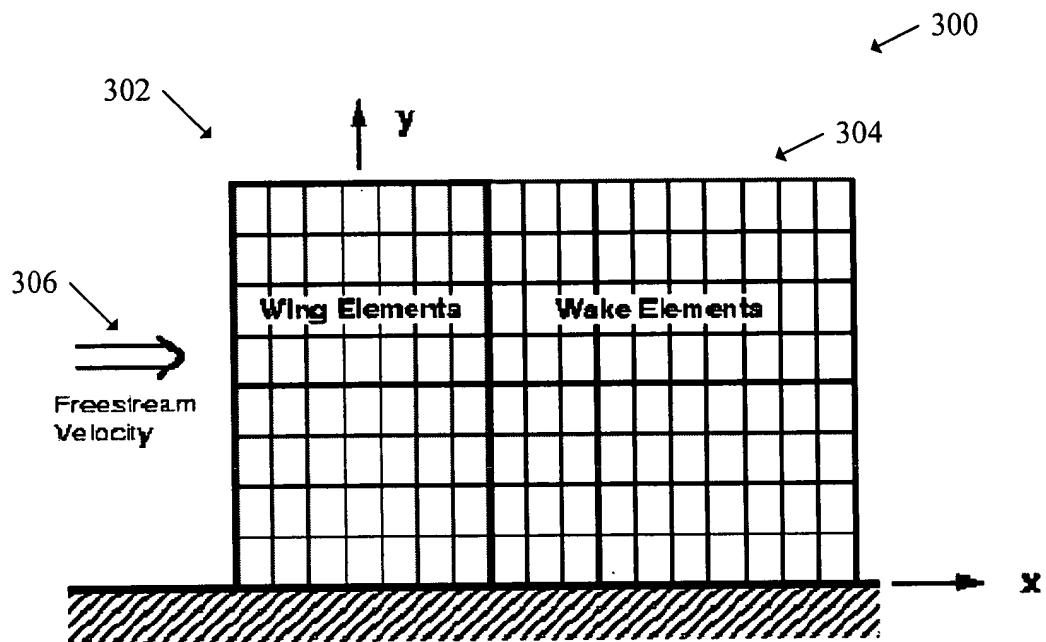


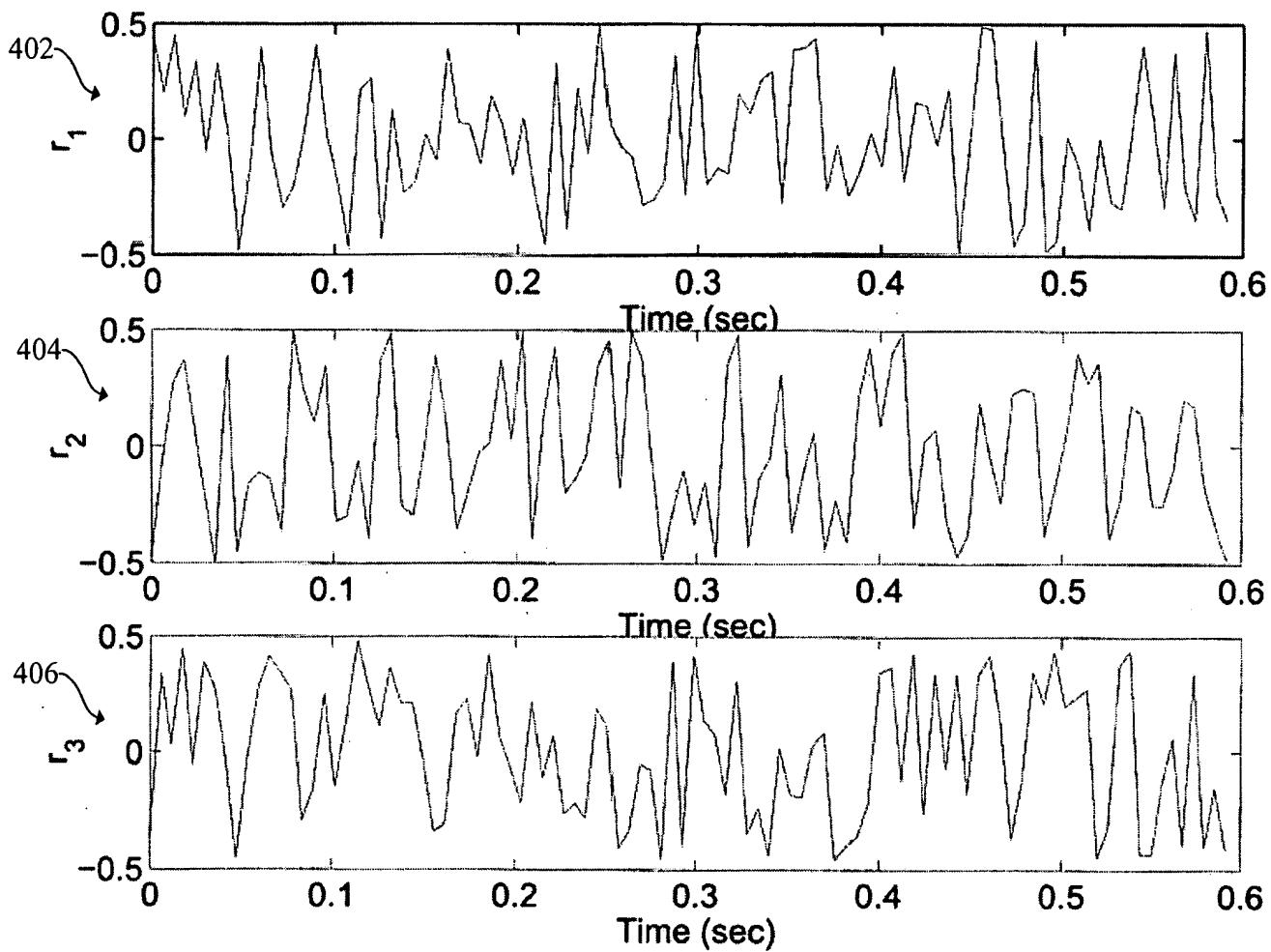
**FIG. 1**  
*(Prior Art)*



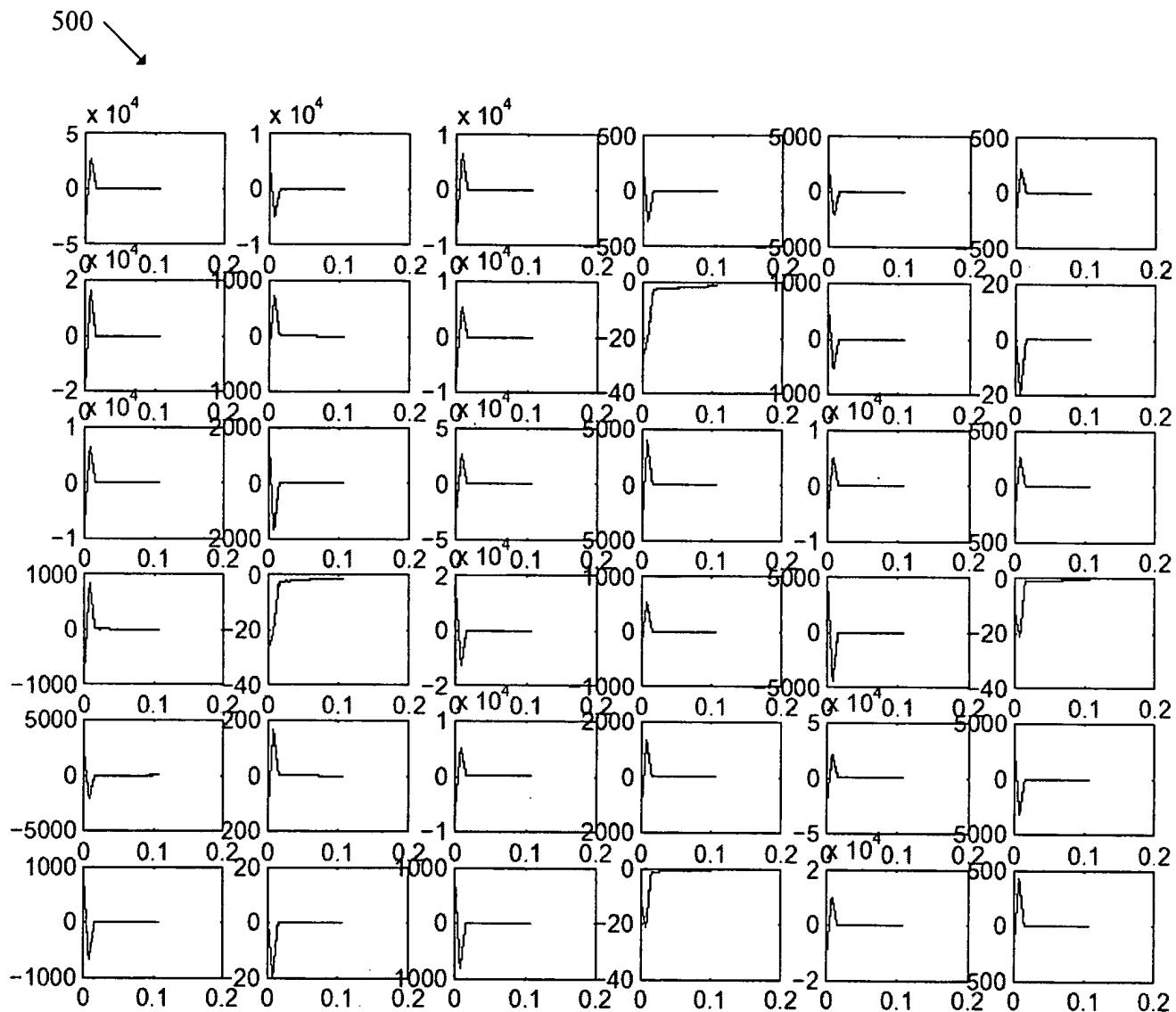
**FIG. 2**



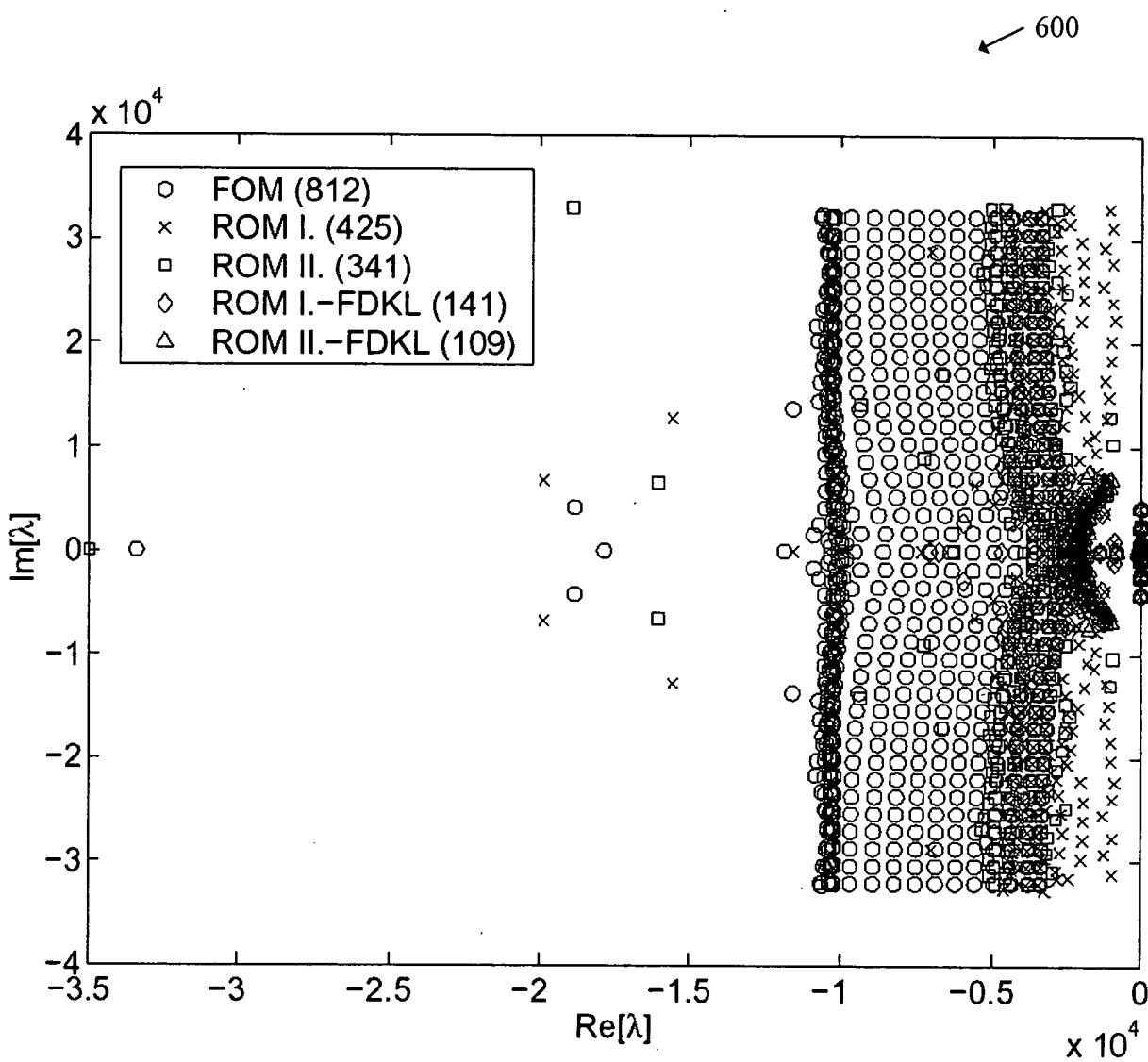
**FIG. 3**



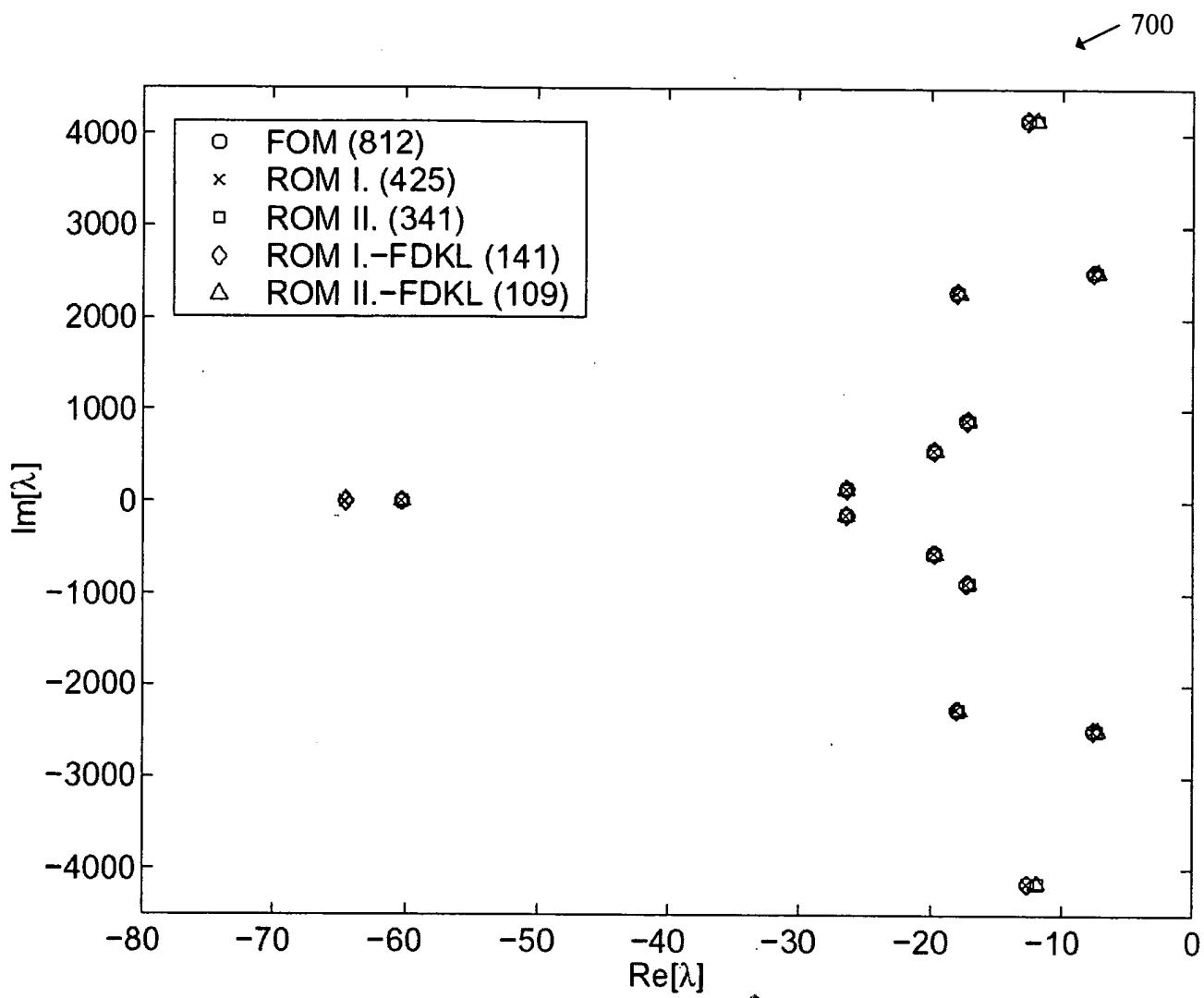
**FIG. 4**



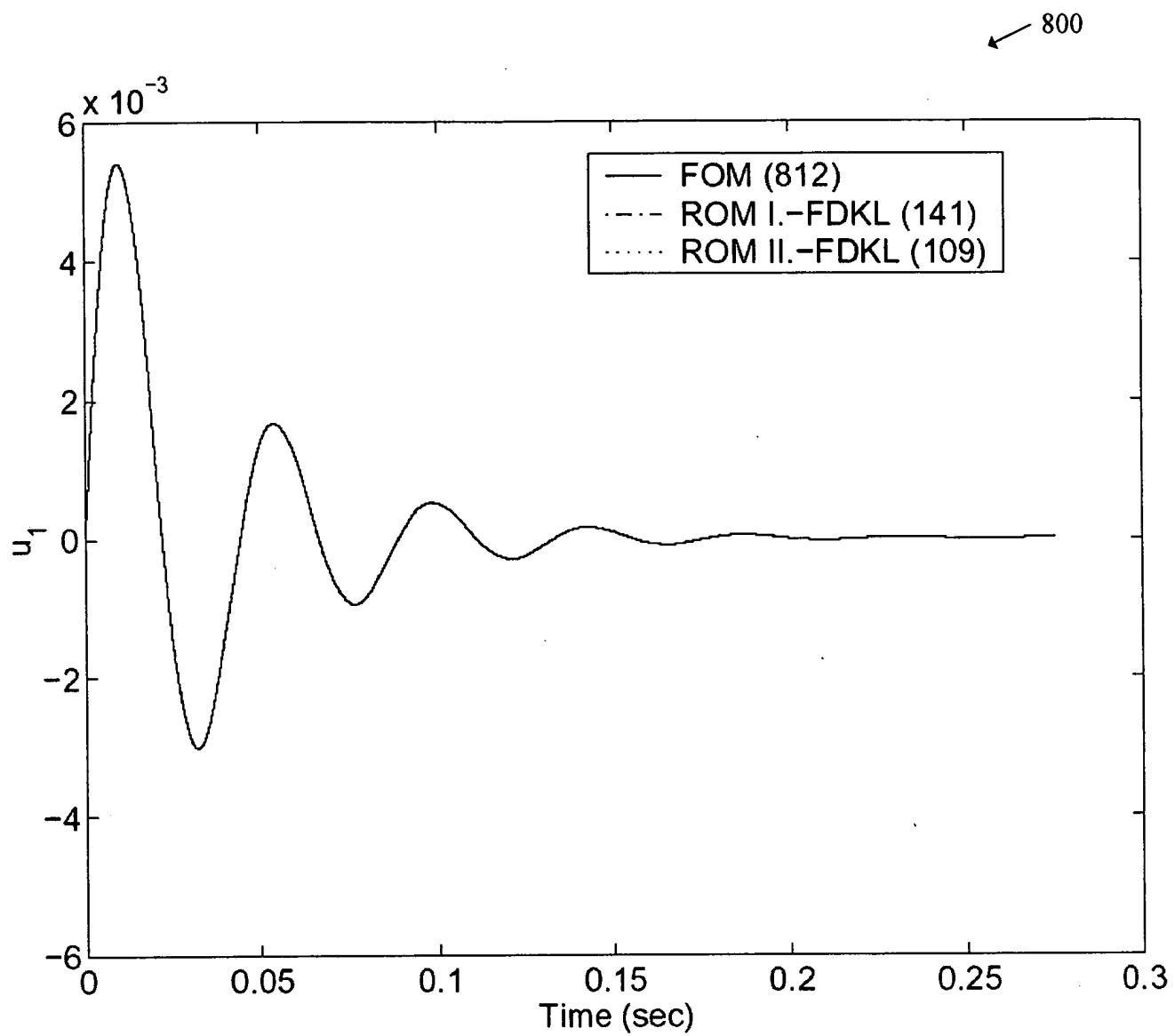
**FIG. 5**



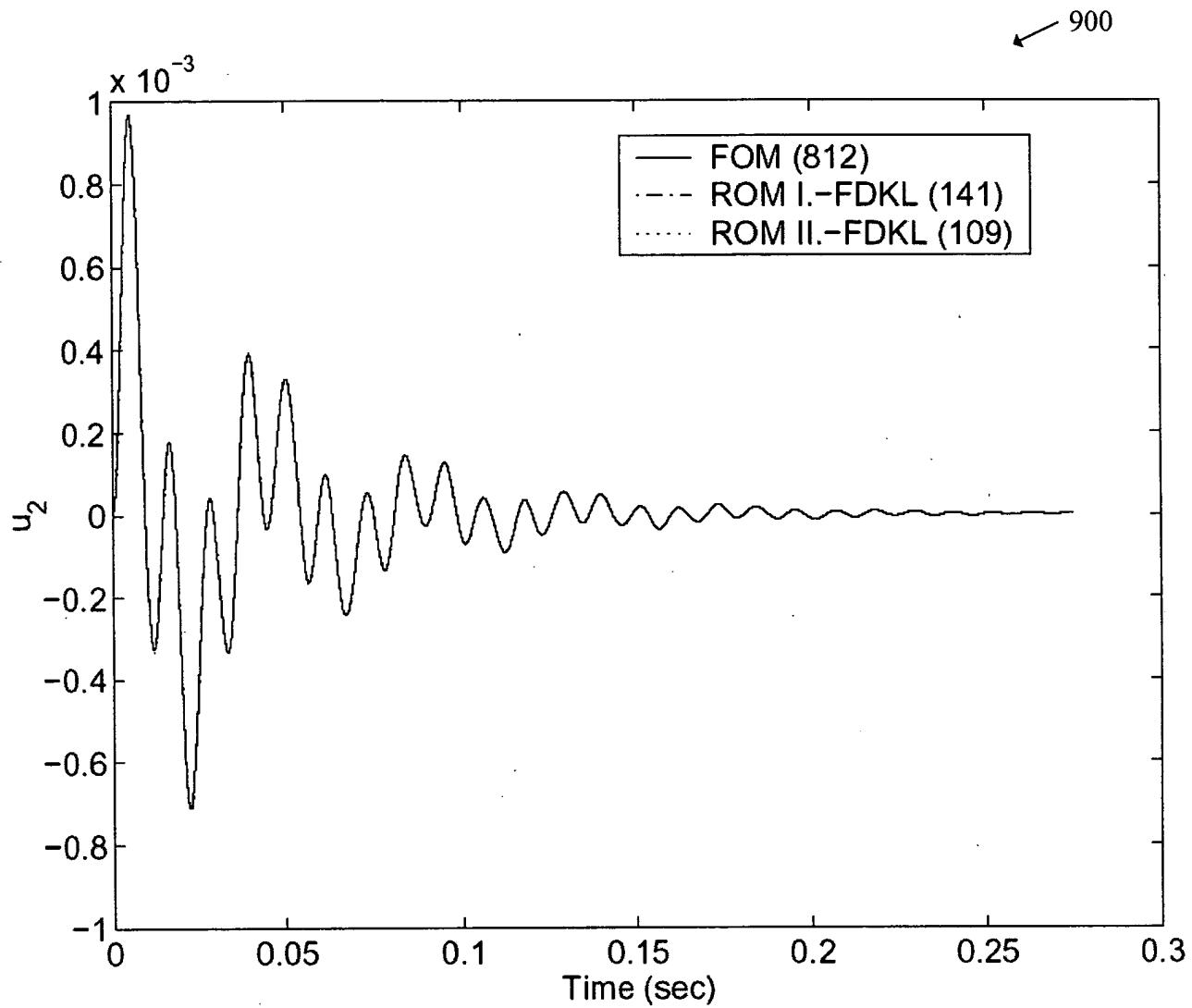
**FIG. 6**



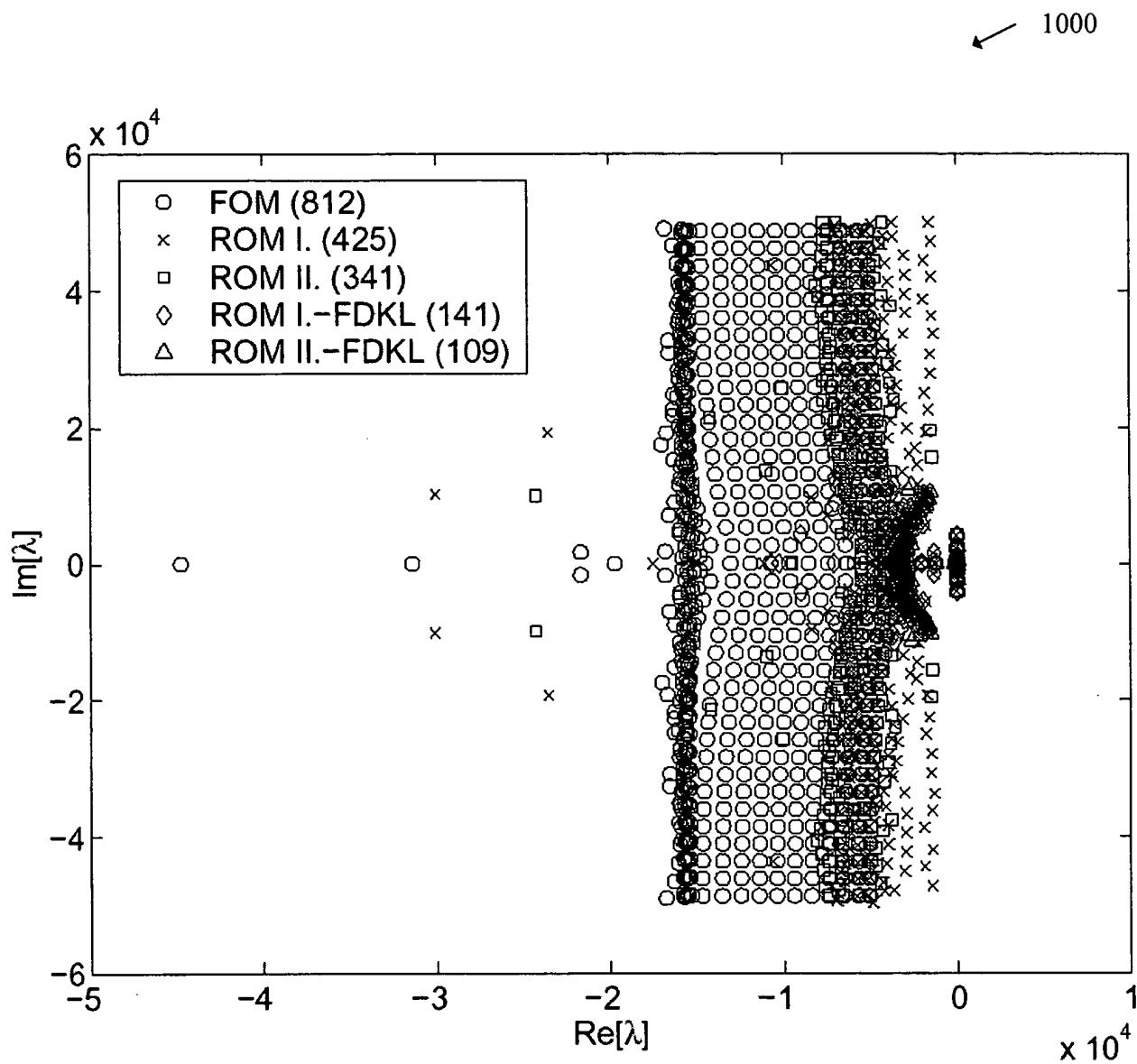
**FIG. 7**



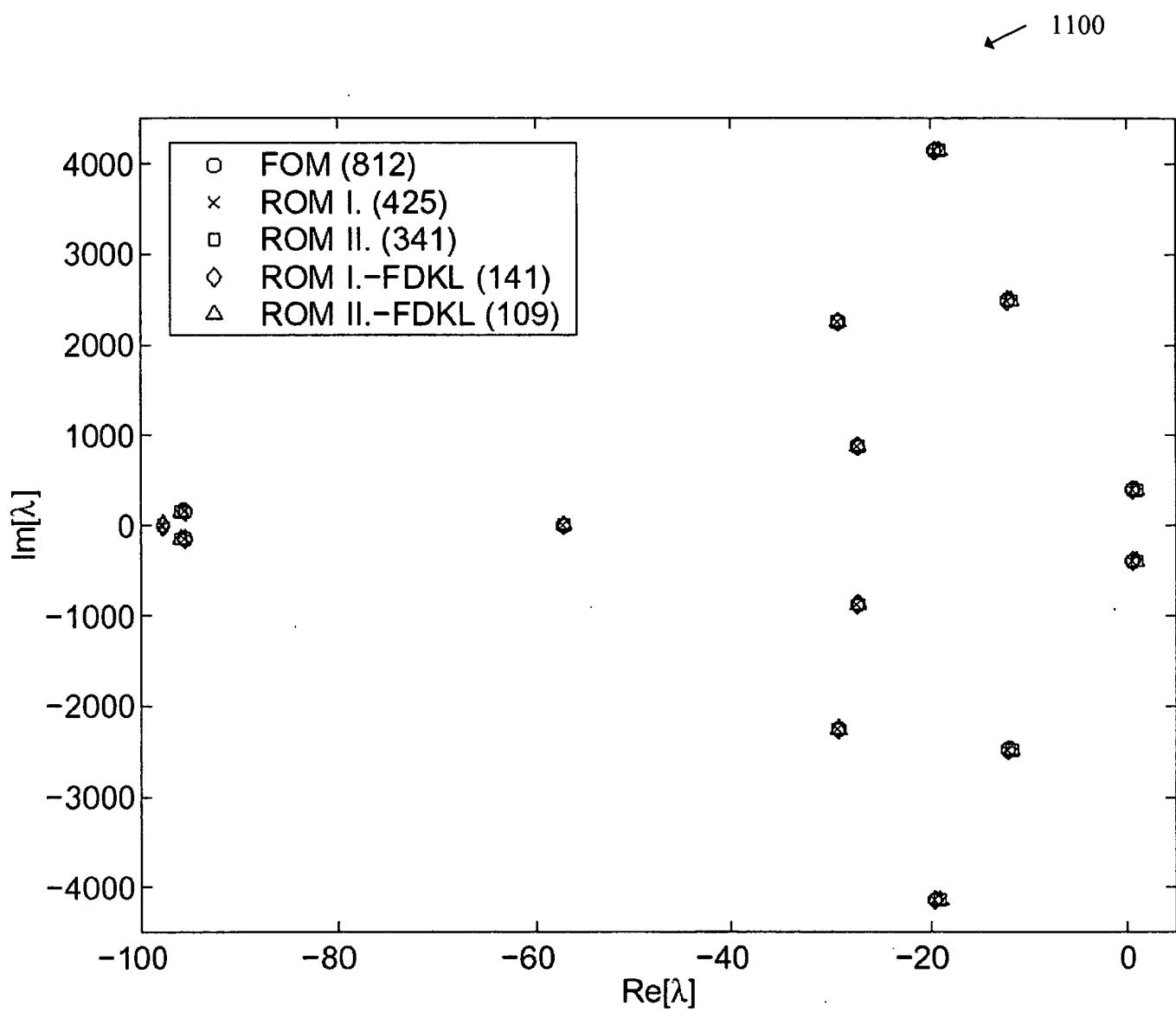
**FIG. 8**



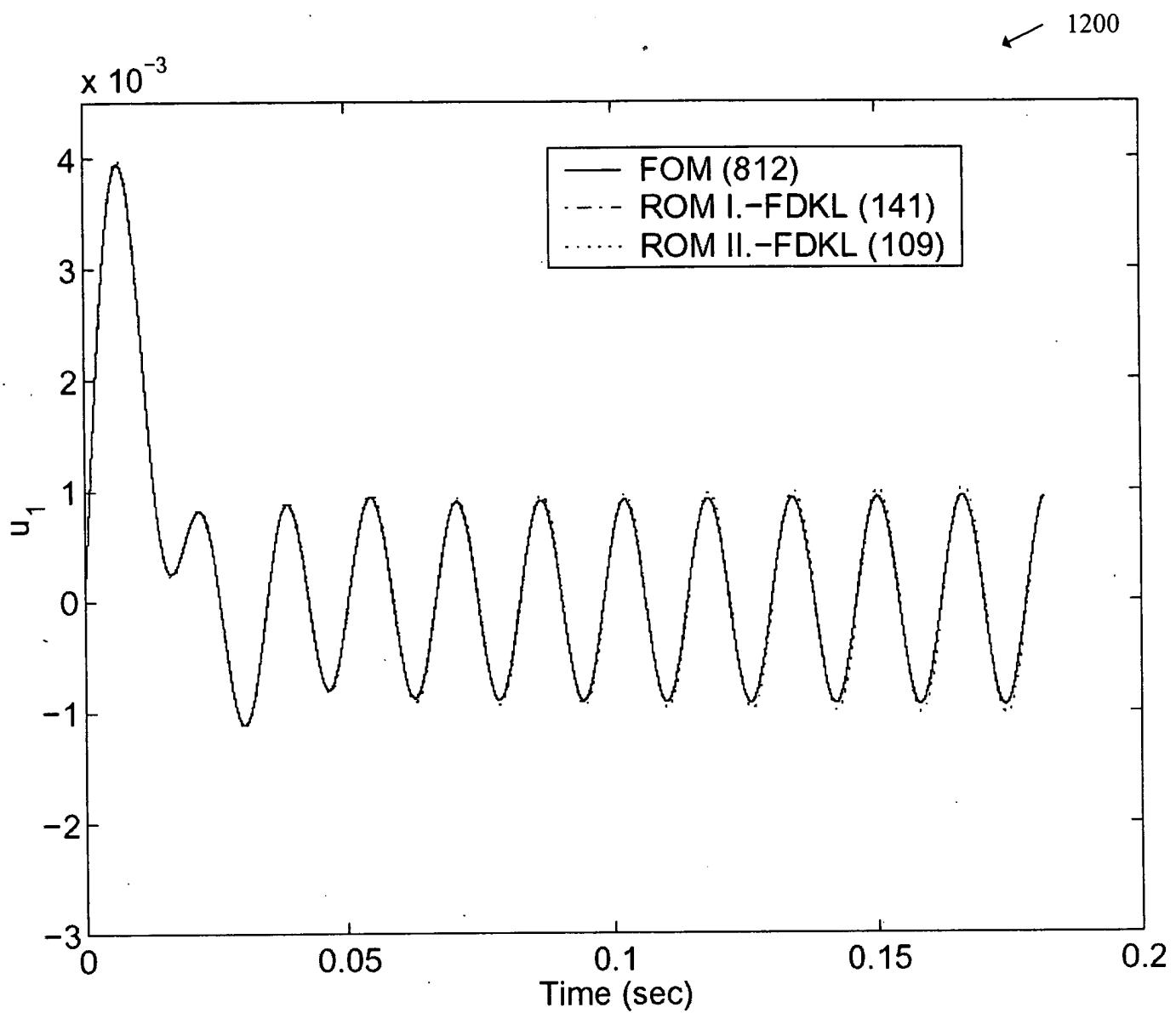
**FIG. 9**



**FIG. 10**

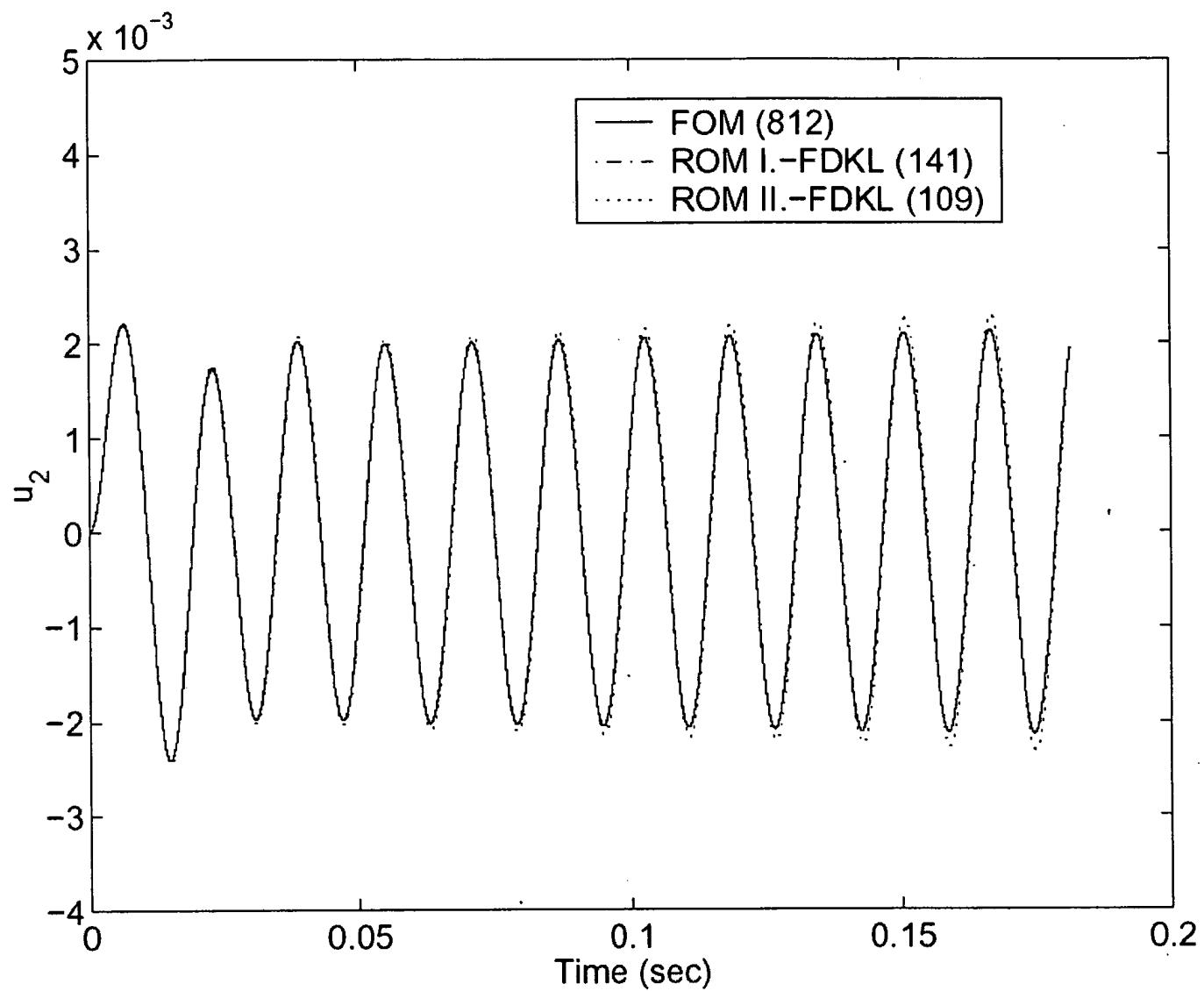


**FIG. 11**

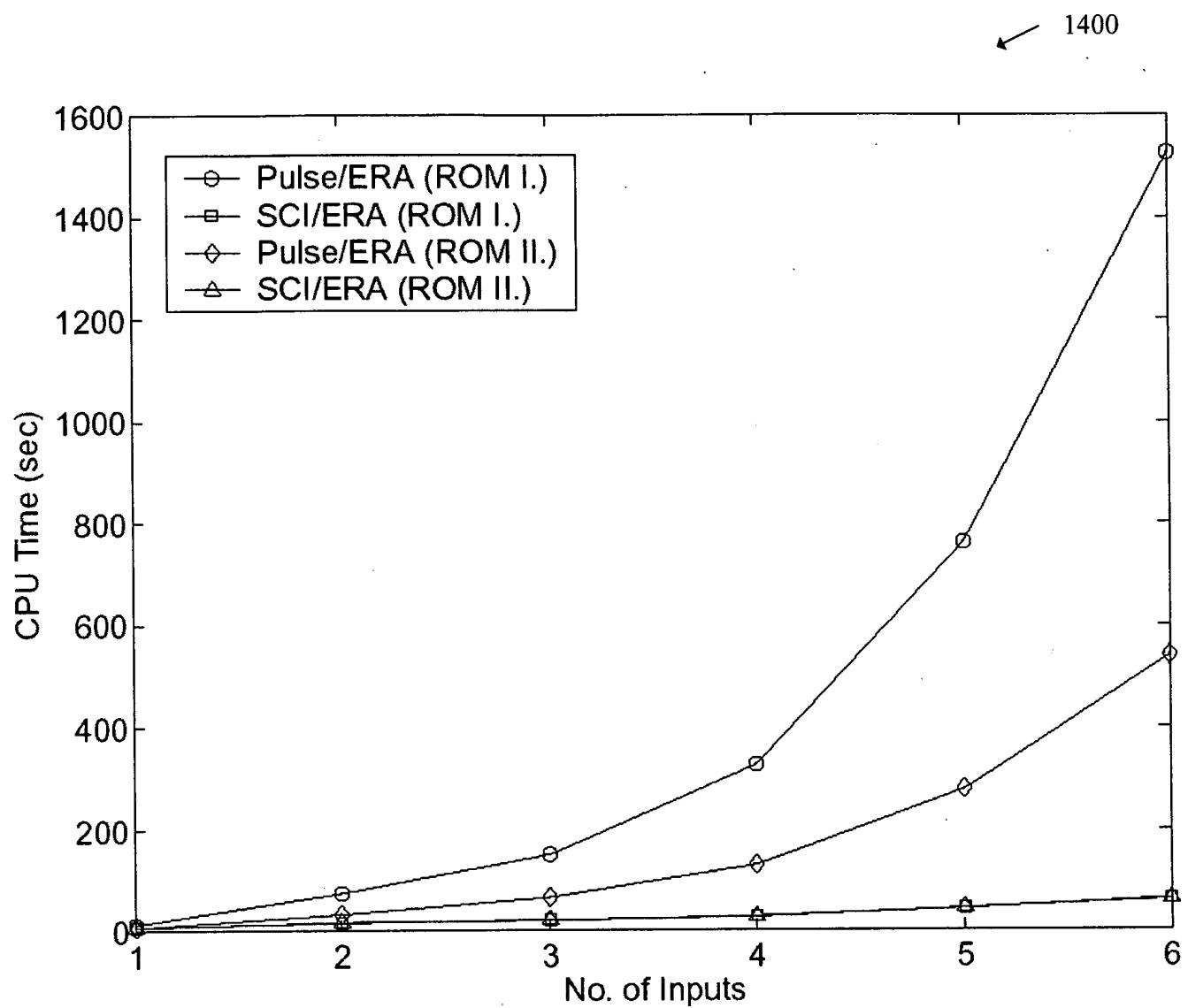


**FIG. 12**

1300



**FIG. 13**



**FIG. 14**

Table 1: CPUs of ERAs Applied to VLM (ROM I.)

$N_i$	Pulse/ERA	SCI/ERA
1	12.3 sec (92)	6.7 sec (89)
2	74.8 sec (180)	16.6 sec (182)
3	150.8 sec (221)	20.6 sec (226)
4	327.8 sec (297)	28.2 sec (298)
5	762.3 sec (336)	43.7 sec (340)
6	1,525.5 sec (395)	63.2 sec (413)

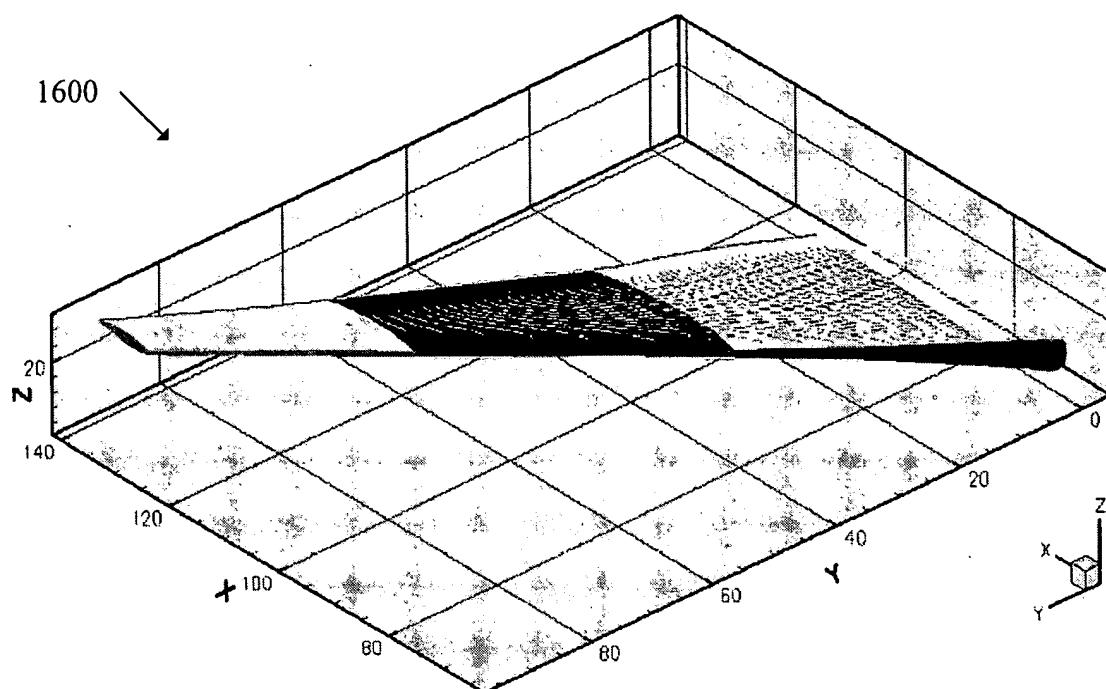
NOTE: Number in ( ) is the size of ROM.

Table 2: CPUs of ERAs Applied to VLM (ROM II.)

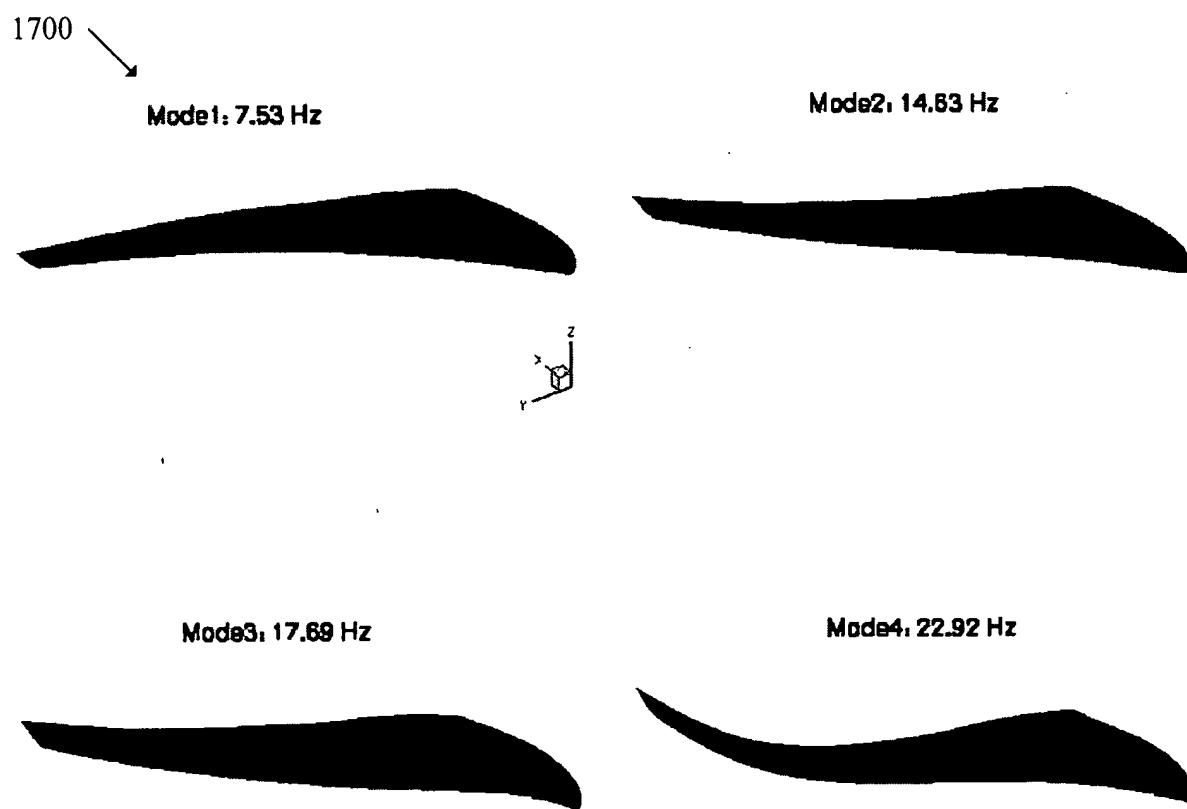
$N_i$	Pulse/ERA	SCI/ERA
1	6.3 sec (92)	6.8 sec (89)
2	32.8 sec (169)	17.00 sec (167)
3	65.9 sec (215)	21.0 sec (214)
4	130.1 sec (258)	27.6 sec (257)
5	279.6 sec (304)	44.1 sec (305)
6	540.4 sec (316)	61.4 sec (329)

NOTE: Number in ( ) is the size of ROM.

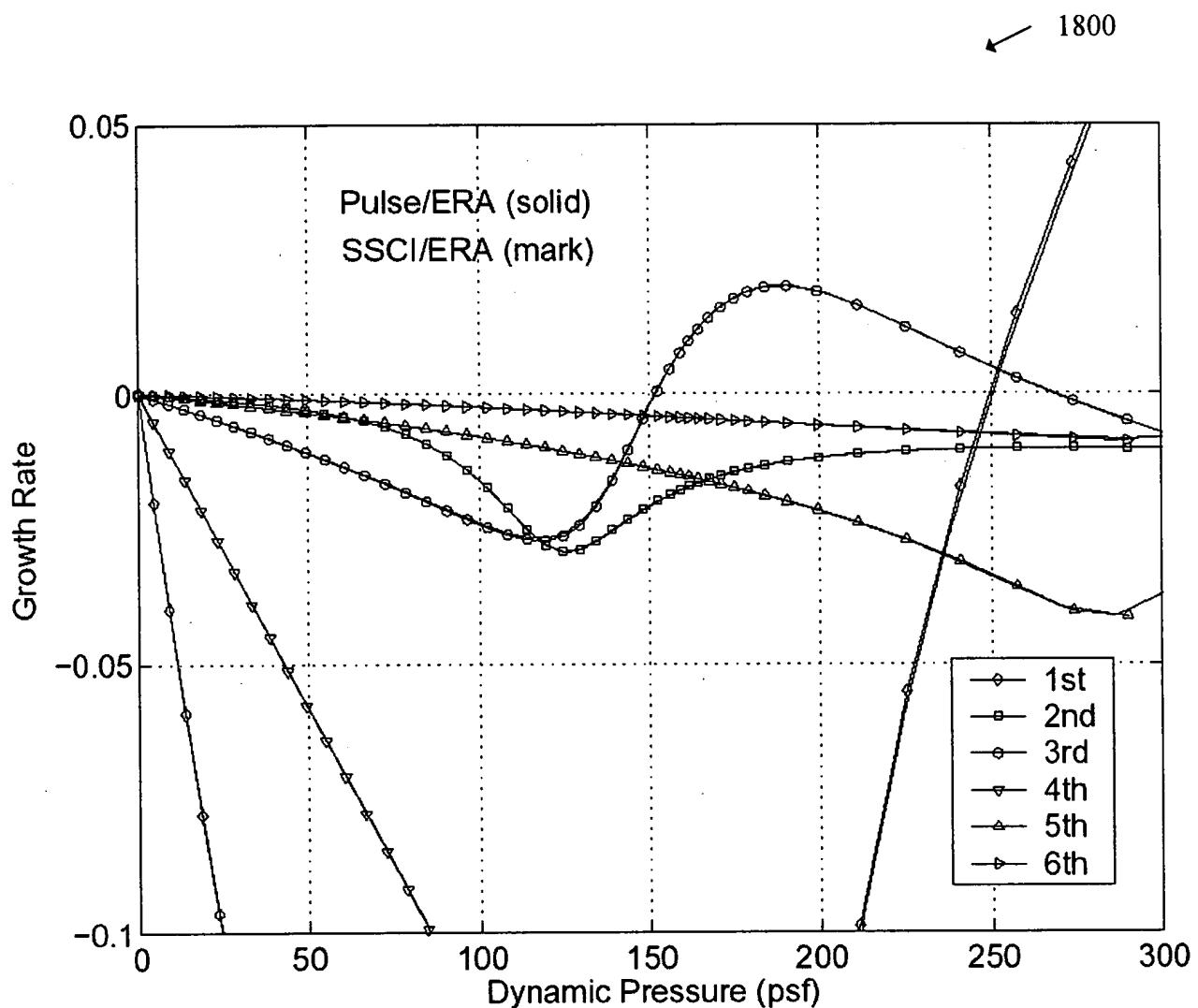
**FIG. 15**



**FIG. 16**



**FIG. 17**



**FIG. 18**